Certification Course

On

PCB Design

Coordinator: Sri K.Kalyan Kumar

Date(s) of Event : 17/05/2021 – 22/05/2021

Organizing department:

Electrical and Electronics Engineering

K.S.R.M.COLLEGE OF ENGINEERING

(UGC-AUTONOMOUS)

Kadapa,Andhra Pradesh,India–516 005

Approved by AICTE, NewDelhi & Affiliated to JNTUA, Ananthapuramu

Cr./KSRMCE/(Department of EEE)/2020-2021 Date: 10/05/2021

To

The Principal,

KSRM College of Engineering,

Kadapa.

Respected Sir

Sub: KSRMCE-(Department of EEE) permission to conduct certification course on

"PCB Design"Request-Regd.

It is brought to your kind notice that, with reference to the cited, the EEE department is planning to conduct Certification Course on " PCB Design " for B.Tech VIII Sem from 17/05/2021 - 22/05/2021. In this regard I kindly request you to grant permission to conduct the certification course. This is submitted for your kind perusal.

Thanking you sir,

Forwarded to principal sir

HEAD
Department of Electrical & Electronics Engineering
K.S.R.M. College of Engineering
Cuddapah - 516 003

Yours Faithfully

Sri K.Kalyan Kumar

Asst.Prof,Dept.EEE

KSRMCE,Kadapa.

To the Director for Information

To All Deans/HoD's/IQAC

Permitted

V. PRINCIPAL
K.S.R.M. COLLEGE OF ENGINEERING
KADAPA - 516 003. (A.P.)

K.S.R.M.COLLEGE OF ENGINEERING

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Kadapa,Andhra Pradesh,India–516 005

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Cr./KSRMCE/(Department of EEE)/2020-2021 Date: 12/05/2021

Circular

All the B.Tech VI Sem EEE students are here by informed that department of EEE is going to conduct certificate course on""PCB Design" interested students may register their names on or before 14, May ,2021 before 5 Pm.

For any queries contact faculty coordinator:

Sri K. Kalyan Kumar, Asst.Prof, Dept. EEE, KSRMCE, Kadapa.

HEAD
Department of Electrical & Electronics Engineering
K.S.R.M. College of Engineering
Cuddapah - 516 003

Head of Department

K.S.R.M.COLLEGE OF ENGINEERING

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Kadapa,Andhra Pradesh,India–516 005
Approved by AICTE, NewDelhi & Affiliated to JNTUA, Ananthapuram

Department of Electrical and Electronics Engineering

Certification Course on "PCB Design"

List of Participants

S.No	Roll Number	Name of the Student	E-Mail Id
1	179Y1A0204	BANDA SIVARAJ	179Y1A0204@ksrmce.ac.in
2	179Y1A0206	BHUMIREDDY CHANDRAKALA (W)	179Y1A0206@ksrmce.ac.in
3	179Y1A0207	DUGGISETTY JAGAPATHI BABU	179Y1A0207@ksrmce.ac.in
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Coordinator

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K.S.R.M. College of Engineering
Cuddapah - 516 003

HOD

Syllabus

PCB Design

Sl. No.	Topic	Hours
		Theory
Module 1	Introduction to Printed circuit board: fundamental of electronic components: Basic electronic circuits, Basics of printed circuit board designing	07
Module 2	Layout planning, general rules and parameters, ground conductor considerations, thermal issues, check and inspection of artwork	07
Module 3	**Design rules for PCB: Design rules for Digital circuit PCBs, Analog circuit PCBs**	08
Module 4	High frequency and fast pulse applications, Power electronic applications, Microwave applications	08

Text Books:

1. Printed circuit Board Design and technology, Walter C. Bosshart

2. Printed Circuits Handbook, Sixth Edition,by Clyde F. Coombs, Jr, Happy T. Holden, Publisher: McGraw-Hill Education Year: 2016

3. Complete PCB Design Using Or CAD Capture and PCB Editor,Kraig Mitzner Bob Doe Alexander Akulin Anton Supon in Dirk Müller, 2nd Edition 2009.

4. Introduction to System-on-Package, Rao R Tummala & Madhavan Swaminathan, McGraw Hill, 2008.

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Approved by AICTE, NewDelhi & Affiliated to JNTUA, Ananthapuram

Department of Electrical and Electronics Engineering

Certification Course on "PCB Design"

Schedule

Timing: 9:00pm – 5:00pm

S.No	Date	Resource Person	Topic Covered
1	17/05/2021	Sri T.Kishore Kumar	Introduction to Printed circuit board: fundamental of electronic components:
2	18/05/2021	Sri T.Kishore Kumar	B asic electronic circuits, Basics of printed circuit board designing
3	19/05/2021	Sri T.Kishore Kumar	Layout planning, general rules and parameters, ground conductor considerations, thermal issues, check and inspection of artwork.
4	20/05/2021	Sri T.Kishore Kumar	Design rules for PCB: Design rules for Digital circuit PCBs, Analog circuit PCBs,
5	21/05/2021	Sri T.Kishore Kumar	High frequency and fast pulse applications
6	22/05/2021	Sri T.Kishore Kumar	Power electronic applications, Microwave applications,

Kalyani
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HoD

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Department of Electrical and Electronics Engineering

Activity Report

Name of the Event	: Certification Course on PCB Design
Date of the Event	: 17/05/2021- 22/05/2021
Scheduled Time	: 9.00 to 5.00PM
Target Audience	: B.Tech VI Sem Students
Student Co-ordinator	:
Venue of the Event	: online (https://meet.google.com/lookup/d3lplbck4s)

Activity Description:

Department of EEE organised a certification course on PCB Design for B.Tech VIII S em EEE Students. Sir has given excellent presentation on PCB Design .Students have done models. With support of head of the department and students the course have been completed successfully.

Coordinator

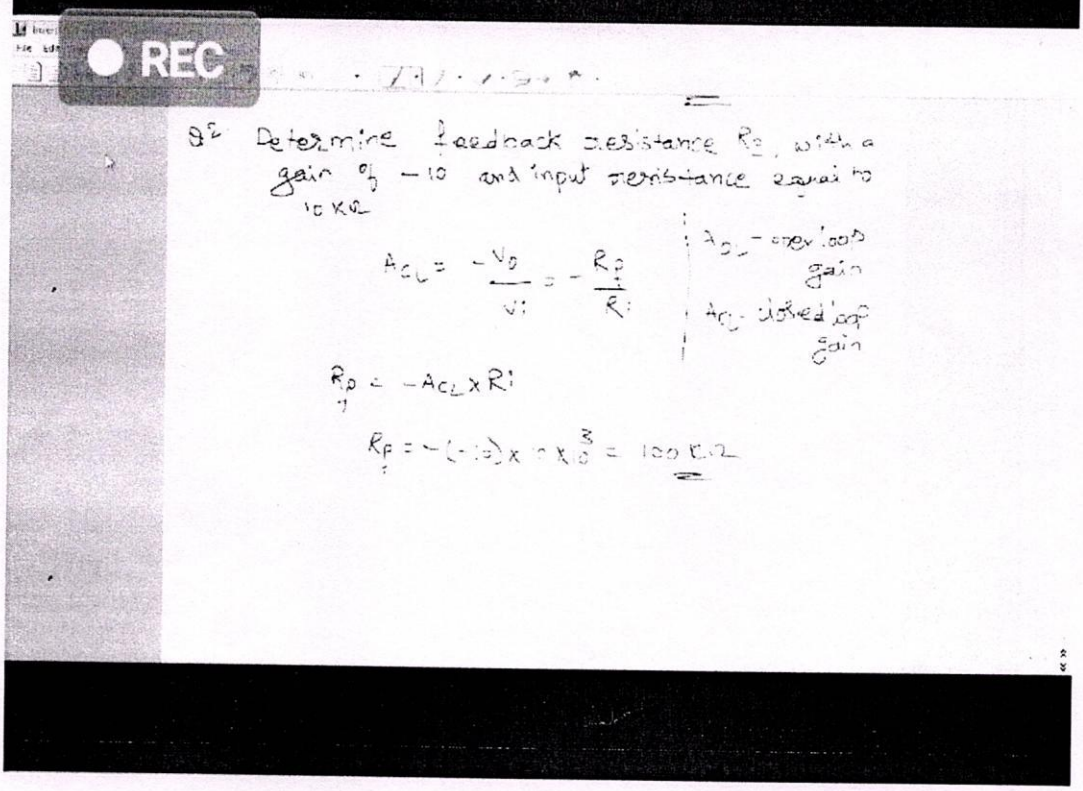
HOD

HEAD
Department of Electrical & Electronics Engineering
K.S.R.M. College of Engineering
Cuddapah - 516 003

Principal

PRINCIPAL
K.S.R.M. COLLEGE OF ENGINEERING
KADAPA - 516 003. (A.P.)

Personal Hotspot : 1 connections, Used 246.17M



(48)

244-SHAIK SAMEER

246 -Sirigireddy Hari...

249-SYED KHAMAR...

251-THUMMALURI JYOT...

KSNR

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Kadapa, Andhra Pradesh, India - 516 003

Certificate Course on

PSB Design
17/05/2021 - 22/05/2021

Organized by

DEPARTMENT OF
ELECTRICAL AND ELECTRONICS ENGINEERING

K.S.R.M.COLLEGE OF ENGINEERING
(UGC-AUTONOMOUS)
Kadapa,Andhra Pradesh,India–516 005
ApprovedbyAICTE,NewDelhi&AffiliatedtoJNTUA,Ananthapuramu.

Department of Electrical and Electronics Engineering
Certification Course on PCB Design - **Attendance Sheet**

S.No	Roll List	Name of the Student	17/5	18/5	19/5	20/5	21/5	22/5
1	179Y1A0204	BANDA SIVARAJ	✓	✓	✓	✓	✓	✓
2	179Y1A0206	BHUMIREDDY CHANDRAKALA (W)	✓	✓	✓	A	✓	✓
3	179Y1A0207	DUGGISETTY JAGAPATHI BABU	✓	✓	✓	✓	✓	✓
4	179Y1A0208	GADDAM ANIL KUMAR	A	✓	✓	✓	✓	✓
5	179Y1A0209	GAJJALAKONDUGARI RENUKA DEVI (W)	A	✓	✓	✓	✓	✓
6	179Y1A0210	GORANTLA SASIDHAR	✓	✓	A	✓	✓	✓
7	179Y1A0211	KRISHNAM SNEHALATHA (W)	✓	A	✓	✓	✓	✓
8	179Y1A0212	KURUBA LAKSHMIKANTH	✓	✓	A	✓	A	✓
9	179Y1A0214	MANCHALA SOWMYA (W)	✓	✓	✓	✓	✓	✓
10	179Y1A0215	MAYANA ABDUL SUHAIB KHAN	✓	✓	✓	✓	✓	✓
11	179Y1A0216	MEDA SANDEEP	✓	✓	✓	✓	✓	✓
12	179Y1A0217	MEKALA GANGADHARA	A	✓	✓	✓	A	✓
13	179Y1A0218	NAKKALAPALLI SHIREESHA (W)	✓	✓	✓	✓	✓	✓
14	179Y1A0219	POSA VENKATA SREEVALLI (W)	✓	✓	✓	✓	✓	✓
15	179Y1A0220	PASUPULETI GAYATHRI DEVI (W)	✓	✓	✓	✓	✓	✓
16	179Y1A0221	RAYAPU VENNELA (W)	✓	✓	A	✓	✓	✓
17	179Y1A0222	SANNAPURI VENKATESH	✓	✓	✓	✓	✓	✓

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20	179Y1A0225	SUCHARITHA PANYAM (W)						
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22	179Y1A0227	SYED HAFEEZ PARVEZ						
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Kalyani
Coordinator

HOD
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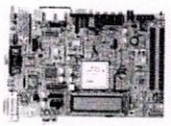
EELE 461/561 – Digital System Design

Module #4 – Interconnect Construction (Printed Circuit Boards)

- **Topics**
  1. Printed Circuit Board Construction
  2. Printed Circuit Board Design
- **Textbook Reading Assignments**
  1. -
- **What you should be able to do after this module**
  1. Describe the fabrication process of a PCB
  2. Design a printed circuit board using modern CAD tools
  3. Understand the signal integrity issues associated with PCBs
  4. Design controlled impedance transmission lines using PCBs
  5. Understand the fabrication limitations of PCBs and how they dictate design rules

Printed Circuit Boards

- **Interconnect (PCBs)**
  - we have examined how parasitics along a Transmission Line can lead to reflections and risetime degradation.
  - now we look at one of the interconnect technologies that is used in modern digital systems.
  - by understanding the manufacturing steps used to create an interconnect, we can understand:
    1) where the electrical parasitics come from
    2) manufacturing limits for *Cost vs. Performance* trade-offs
- **Printed Circuit Boards**
  - a structure that:
    1) mechanically support components
    2) provides electrical conduction paths between circuits



Printed Circuit Boards

- **Terminology**

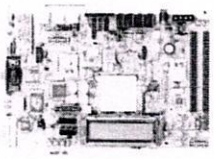
"PCB" = Printed Circuit Board (i.e., a "board")

"PWB" = Printed Wiring Board (same as PCB)

"PCA" = PCB Assembly - a PCB that is loaded with components

"Fab" = the process of creating the PCB

"Load" = the process of attaching the components to the PCB



Printed Circuit Boards

- **Construction**
  - there are a variety of methods to create a PCB.
  - the general approach is to start with a sheet of copper attached to an insulator and then remove copper leaving only your desired interconnect pattern.
  - this is called a *subtractive* method and is the most common technique.
  - we'll first go over all of the major process steps used in creating a PCB.
    1) The CORE
    2) Patterning
    3) Vias
    4) Pattern Plating
    5) Solder Mask
    6) Surface Finish
    7) Silk Screening
  - then we'll put them together in the appropriate sequence from start to finish.

PCB: Core

- **The CORE**
  - the base element to a PCB is called the "CORE"
  - this typically consists of two sheets of thin copper laminated (or glued) to an insulating material.
  - the insulator is commonly call the "Substrate" or the "Laminate"
  - this construction is also called a "Copper Clad" insulator
  - COREs come in large sheets which are typically ~18" x 24" (but can be as large as 24" x 48")

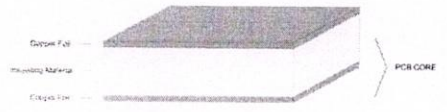
PCB: Core

- **The CORE**

CORE Conductors

- the most commonly used conducting material is *Copper (Cu)*
- the thickness of the copper sheet is specified in terms of its *weight*:

2oz	= 70 um	= 0.0024"	The term "weight" refers to the weight in
1oz	= 35 um	= 0.0012"	ounces per square foot"
0.5oz	= 17.5 um	= 0.0006"	
0.25oz	= 8.75 um	= 0.0003"	We sometimes call this sheet a "foil"



PCB: Core

- **The CORE**

CORE Insulators

- There are many different types of insulating material, each with varying degrees of:
  - Cost
  - Dielectric Constants
  - Electrical Performance (i.e. Dissipation factor = loss tangent)
  - Mechanical Robustness (rigidity, peel-strength, CTE)
- COREs are typically reinforced with a weave of fiber
- FR4 (Fire Retardant Epoxy #4) is the most common dielectric in use today

PCB: Patterning

- **Patterning**
  - there are 2 common techniques to remove material from the core to leave only the desired conduction paths.

1) Photoengraving / Photolithography

- a photomask is created by *printing* a design pattern onto a translucent material.
- this is very similar to printing an overhead transparency using a laser printer.
- the CORE is then covered in a photosensitive material (photosensitive dry film, or photoresist).
- when the photosensitive material is exposed to light, its properties change.

PCB: Patterning

- **Patterning**

1) Photoengraving / Photolithography cont...

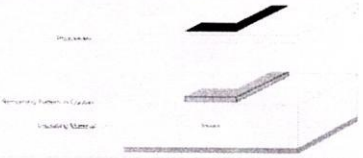
- the CORE is ***exposed*** to a light source through the photomask
- a solution is then applied that ***develops*** the photosensitive material making it soluble

PCB: Patterning

- **Patterning**

1) Photoengraving / Photolithography cont...

- an *etching* solution is then applied to the CORE which removes the *"now soluble"* photosensitive material in addition to the copper foil beneath it.
- this etching step removes any copper on the CORE that was exposed to light through the photomask, thus transferring the pattern.
- once the remaining photosensitive material is ***stripped*** using a cleaning solution, the CORE is left with a pattern of copper identical to the pattern on the photomask.



PCB: Patterning

- **Patterning**

2) PCB Milling

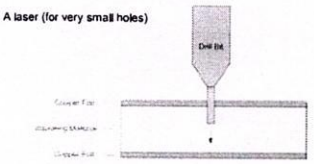
- another subtractive technique is to use a milling bit (similar to a router or drill bit) to mechanically remove copper from the CORE leaving only the desired pattern
- we have one of these machines at MSU

PCB: Vias

- **Vias (Drilling)**
  - A via is a structure that electrically connects two different layers of copper in a PCB.
  - the first step in creating a via is to drill a hole where the contact will be made.
  - this can be done using:
    1) A mechanical process (i.e., a regular drill bit). This is currently the most common approach.

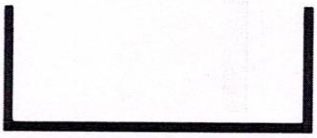
       or

    2) A laser (for very small holes)



PCB: Vias

- **Vias (Electroless Plating)**
  - The next step in creating a via is to deposit Copper into the holes in order to **Plate** the inner diameter of the via with a conducting material.
  - PCB Via plating is accomplished by an *Electroless Plating Process* in which a series of chemical reactions are performed to transfer copper atoms from a *Sacrificial Copper Source* to the barrels of the via holes.



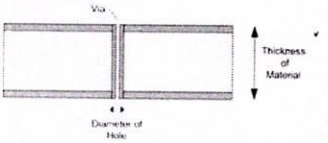
NOTE

'Electroplating' is where the metal source is ionized and drawn to the target using an electric field.

'Electroless Plating' uses a chemical reaction to release hydrogen from the target in order to create a negative charge and attract the plating metal to its surface.

PCB: Vias

- **Vias**
  - The end result is a structure that connects different layers of a PCB.
  - The "via" is also called a "Plated Through Hole"



NOTE The **Aspect Ratio** is the ratio of the *Thickness of the Hole* (or Depth) to be plated to the *Diameter of the Hole*. If the aspect ratio is too large (i.e., deep & skinny holes), then the copper plating will not reach the center of the hole and result in an open circuit.

$$\text{Via Aspect Ratio} = \frac{Depth}{Diamter}$$

PCB fab shops will specify the maximum aspect ratio they can achieve (typically ~4-6)

PCB: Pattern Plating

- **Pattern Plating**
  - the copper deposited from the *Electroless Plating* step applies a thin layer of copper on the entire surface of the CORE in addition to inside the drilled via holes.
  - the plating in the via barrels is typically not thick enough (i.e., <0.001") to be reliable. To address this, a second *Electrochemical* plating is performed.
  - *Pattern plating* deposits a material over the copper circuitry that will protect it during a subsequent etch stage. A material such as *tin* can be used to cover the copper traces to protect them.
  - the copper is first thickened using an additional *Electrochemical* plating process.
  - once applied, the tin is deposited on the pattern.
  - after the etch, the tin can be *stripped* off or left on depending on the manufacturer.

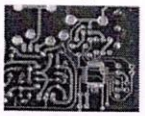
PCB: Solder Mask

- **Solder Mask**
  - solder mask is a protective insulating layer that goes over the outer sides of the PCB.

    NOTE: this is typically the *green* material you see on boards.
  - copper is very susceptible to oxidation so if the pattern is going to be exposed to ambient air, they need to receive additional plating to protect against oxidation.
  - oxidation is the reaction of oxygen with the copper. During this process, the copper is actually *consumed*. So a thin layer of copper can actually be completely oxidized into an insulator.
  - solder mask is a layer of polymer that can be applied using either *silk screening* or a spray.
  - the solder mask covers all conducting circuits on the board with the exception of any *pads* that components will connect to.

NOTE: The word *pad* has special meaning in PCBs. It indicates that a shape of metal

1) will be used to connect to a component
2) will not be covered by solder mask
3) will receive a surface finish (next step)
4) will receive a layer of solder paste prior to component loading (later)

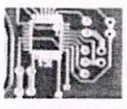


PCB: Surface Finish / Solder Coat

- **Surface Finish**
  - also referred to as Solder Coat or Exposed Conductor Plating
  - the *pads* of a board must receive a special surface finish to

    1) resist oxidation from long periods of storage while waiting for loading
    2) prepare them for the application of solder
  - to accomplish this, a layer of conducting material is applied to the pads after solder masking.

    Ex) Tin-Lead Solder (industry is trying to move to "lead free" plating)
    Gold
    Silver (Lead-Free compliant, ROHS)
  - this step is what gives the pads on the board the *shiny* look that you see.

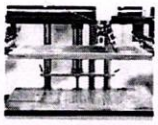


PCB: Silkscreen

- **Silk screening**
  - silk screening is the process of adding documentation to the board.
  - the term *silk screen* refers to the process of transferring a pattern using a special *stencil*.
  - a *stencil* is a sheet of material that has physical openings in it that represent the pattern to be transferred.
  - in a silk screen stencil, the openings are typically a set of small dots (i.e., a *screen*)
  - the stencil is laid on top of the board and then a documentation material is applied to the entire board using a roller & *squeegee* or *spray*.
  - when the stencil is removed, the documentation material remains in the pattern of the openings on the stencil.
  - the board is then baked to harden the documentation material.

PCB: Silkscreen

- **Silk screening**
  - you typically cannot draw silk screen lines that are smaller than the copper due to the resolution of the screening process
  - when looking at how small of a line can be drawn using a silk screen, manufacturers typically talk about LPI (lines per inch). In general, the smallest silk screen lines are ~0.008"

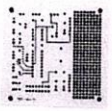


silk screen machine

patterns remaining after silk screen

2 Layer PCB Example

- **Step 1 – Photomask**
  - we create our design in a CAD tool (i.e., Mentor PADS) which generates files to create a photomask



- **Step 2 – Material Selection**
  - we now select a core that meets our application needs (Dk, loss tangent, copper weight, etc...)
  - this core will be used to create our PCB.

2 Layer PCB Example

- **Step 3 – Drilling**
  - we now drill through holes where vias are going to be located

- **Step 4 – Electroless Plating of Vias**
  - we now put the board through an Electroless plating process which deposits copper inside of the via drill holes

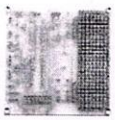
2 Layer PCB Example

- **Step 5 – Apply Pattern**
  - we now transfer the pattern from our photomask to the core by:
    - applying photosensitive film (photo resist) to the CORE.
    - align photomask to the CORE
    - expose to UV light which changes the properties of the exposed photo resist
    - apply developing solution to make the exposed photoresist soluble

- **Step 6 – Pattern Plating**
  - since the current copper patterns are going to be on the outer sides of the board, they require additional steps to ensure that oxidation doesn't completely consume the metal.
  - the board undergoes an additional electrochemical plating step that adds additional copper to the existing copper traces and via barrels.
  - a layer of tin is then added to the surface to protect the copper from the ensuing etch.

2 Layer PCB Example

- **Step 7 – Strip & Etch**
  - we now strip the photo resist layer off of the core exposing the unwanted copper
  - an etch is performed which removes all of the unwanted copper
  - the copper circuitry is protected by the tin and remains after the etch.



- **Step 8 – Solder mask**
  - an insulating layer of solder mask is applied to the core.
  - the solder mask covers all of the conductors with the exception of any pads that are to be used to connect to components.
  - this layer provides protection against inadvertent shorting of the conductors

2 Layer PCB Example

- **Step 9 – Surface Finish**
  - the pads that are visible through the solder mask will ultimately make contact to components using solder.
  - In order to prepare the pads for the components, a layer of material is applied to the pads that:
    - is easily soldered to (i.e., Solder, Gold, or Silver)
    - that prevents any oxidation on the pads so that the board can be stored while waiting for load.

- **Step 10 – Silk Screen**
  - documentation is now added to the board using a silk screen material.
  - documentation is important for:
    - board identification
    - component locators
    - component orientations

2 Layer PCB Example

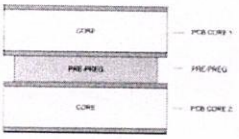
- Step 11 – De-Panelization
  - Typically, multiple images of the same PCB are put on one panel for processing
  - this allows the previously described process steps to create multiple boards in the same amount of time
  - the last step is to *de-panelize*, or route out the individual boards

NOTE: Some automated loading processes can load the boards while still panelized

Multi Layer PCBs

- Multi Layer PCBs
  - the same set of steps can be used to create PCB's with more than 2 layers.
  - in this case, multiple cores are patterned and then *laminated* together using an insulator material called a *pre-preg*
  - the pre-preg serves as an insulator but has an adhesive property to it that *glues* the cores together.
  - the pre-preg material can be the same insulating material as the core.

NOTE: this construction process is why boards always come with an EVEN number of layers (i.e., 2 layer, 4 layer, 6 layer, 8,...)



Multi Layer PCB

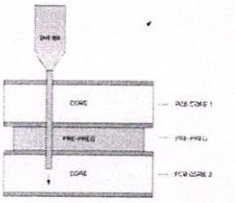
Multi Layer PCBs

- Multi Layer PCBs
  - the resultant *stack* of layers is called a "stackup"
  - outer layers can be added to the stack by applying a pre-preg to the core and then laminating a copper foil on top of it
  - the entire stack (core + pre-pregs) are put into a press
  - the press applies pressure and temperature in order to bond the materials together into one rigid assembly

4 Layer PCB

Multi Layer PCBs

- Multi Layer PCBs
  - creating multi-layer PCBs involves some changes to the fabrication process.
    1) Drilling occurs after the final lamination takes place.
    2) The inner layer traces are patterned prior to drilling and lamination and DO NOT need to undergo the pattern plating and surface finish step.
  - notice that the through-hole vias will extend through the entire thickness of the board even if the desired connectivity is between the top two layers.



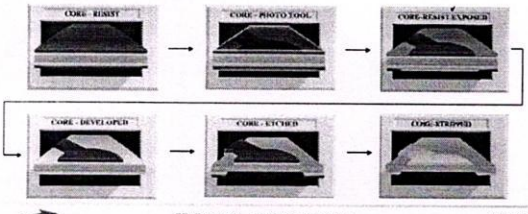
4 Layer PCB Example

- Step 1 – Photomask
  - we need to create photo masks for each layer in the design
  - for a 4 layer board, we need to have photo masks for each of the 4 metal layers in addition to misc layers (s&k, mask, etc.. more on this later)

- Step 2 – Material Selection
  - for a 4 layer board, we will use one CORE for the inner layers and then *laminate* foils to the top and bottom to form the outer layers.

4 Layer PCB Example

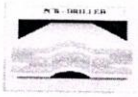
- Step 3 – Inner Layer Patterning
  - we now fully pattern the inner layers of the PCB.
  - this step is slightly different from a 2 layer PCB because these traces will not be on the outside of the board so they aren't susceptible to oxidation (i.e., no need for pattern plating).
  - in addition, since there will no components contacting these layers, there is no need for a surface finish or solder mask.



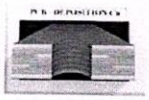
4 Layer PCB Example

- **Step 4 – Lamination**
  - now a pre-preg material is applied to both sides of the CORE and foil is *laminated* on both sides.
  - this stack is put into a press to apply pressure and temperature in order to bond the foils to the CORE

- **Step 5 – Through Hole Drillings**
  - the entire stack is drilled



- **Step 6 – Electroless Plating of Vias**
  - the drill holes are then plated with copper using an Electroless plating process

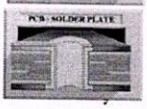


4 Layer PCB Example

- **Step 7 – Apply Pattern**
  - the outer layers are now coated with photoresist and the pattern is transferred using the outer layer photo masks.

- **Step 8 – Pattern Plating**
  - the board undergoes an additional electrochemical plating step that adds additional copper to the existing copper traces and via plating.

  - a layer of tin (or solder) is then added to the surface to protect the copper from the ensuing etch.



4 Layer PCB Example

- **Step 9 – Strip & Etch**
  - we now strip the photo resist layer off of the core exposing the unwanted copper
  - an etch is performed which removes all of the unwanted copper
  - the copper circuitry is protected by the tin (or solder) and remains after the etch
  - the entire surface is then stripped leaving only the desired pattern in copper

4 Layer PCB Example

- **Step 10 – Solder mask**
  - now a solder mask is applied over the outer layers leaving openings for the pads to which components will be soldered.
  - "SMOBC" stands for "Solder Mask Over Bare Copper" and refers to a process in which the tin pattern plating was removed.

- **Step 11 – Surface Finish**
  - now the pads are coated with a material that protects them from oxidation and allows them to be easily soldered to.
  - "HAL" stands for "Hot Air Surface Level" (aka HASL) and refers to a process of adding solder to the surface of the board using hot air to *melt and blow* the solder onto the pads.

  - a more modern process is called *Emersion Silver* and refers to dipping the board in Silver. This process is Lead-Free.

4 Layer PCB Example

- **Step 12 – Silk Screen**
  - lastly, documentation is added to the outer layers of the boards

- **Step 13 – De-panelization**
  - if multiple images were fabricated on the same panel, then the boards are now routed into individual boars

PCB CAD

- **CAD = Computer Aided Drawing**
  - a PCB CAD tool allows us to enter our design and ultimately produce information that a PCB Fab shop can use to create the PCB.
  - the files that the tool produces are called "Computer Aided Manufacturing (CAM) files.
  - the design flow for PCB CAD consists of:

1) Part Library Development	- A library contains all of the parts in your design. Each part contains a schematic, a physical layout, and information about the vendor that can be used to create a "Build of Materials"
2) Schematic Entry	- A schematic contains all of the part symbols and how they are connected. "Parts" will drive forward the pad configuration in the layout and "*nets*" will drive forward the traces and plane shapes.
3) Layout	- A physical layout is then performed in which all of the parts are placed and connected with traces.
4) CAM	- The final step is to create the Gerbers, Drill Files, and Drawings to be sent to the fab shop.

PCB CAD (GERBER)

- **GERBERs**
  - in the PCB CAD tool, each design image is assigned a *Layer*
  - every metal layer will be assigned its own layer.
  - layers are numbered in ascending order from top to bottom (ex. L1, L2, L3, L4)
  - layers are also used to describe the top and bottom side *Solder Mask*
  - layers are also used to describe the top and bottom side Silk Screen
  - the CAM files from the CAD tool are produced in an industry standard format called **GERBER**
  - extensions for GERBERS can be * GBR, * PHO, * ART (Mentor Pads uses * PHO)
  - a GERBER file describes the image patterns that are present on that layer
  - an "*aperture*" file is a way to describe to the photo plotting machines how to interpret the shapes described in the GERBER

NOTE the term *Gerber* comes from a standard format for photo plotters published by the *Gerber Systems Corporation* in 1980

PCB CAD (GERBER)

- **GERBERs**
  - each layer in the design will produce its own GERBER file.

Ex) for a 4 layer board, we will have:

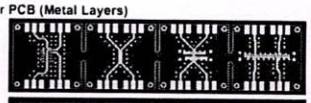
L1.pho
L2.pho
L3.pho
L4.pho
top_silk.pho
top_mask.pho
bottom_silk.pho
bottom_mask.pho

aperture_report.rep

PCB CAD (GERBER Example)

- **Example : GERBERS for a 4 layer PCB (Metal Layers)**

L1.pho



L2.pho
(this layer is a ground plane)

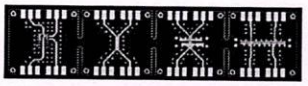
L3.pho
(this layer is a ground plane)

L4.pho

PCB CAD (GERBER Example)

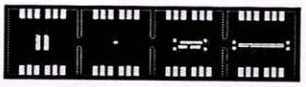
- **Example : GERBERS for a 4 layer PCB (Top Silk & Top Mask)**

L1.pho
(shown again for reference)



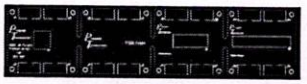
top_mask.pho

-note that this layer is *negative*, meaning that the shapes represents where mask will NOT be



- note that every pad on L1 must have a solder mask opening so that components can make contact.

top_silk.pho



PCB CAD (GERBER Example)

- **Example : GERBERS for a 4 layer PCB (Bottom Silk & Bottom Mask)**

L4.pho
(shown again for reference)

bottom_mask.pho

-note that this layer is *negative*, meaning that the shapes represents where mask will NOT be

-note that every pad on L4 must have a solder mask opening so that components can make contact

bottom_silk.pho

this board didn't have any silk screen on the bottom

PCB CAD (Drill Data)

- **Drill Data**
  - information for drill sizes and locations are contained within a separate set of files.
  - these files are called "Numerically Controlled Drill (NCD) Files" or "Excellon" files.
  - the information in these files is a list of XY coordinates for where each drill hole will be made.

Ex) for a 4 layer board done in Mentor PADS, we generate

drill.drl : the NCD drill file that is read by the drilling machine
drill.lst : a list of drill coordinates in a user-friendly format for manual checking
drill.rep : a list of all drill sizes in a user-friendly format for manual checking

PCB CAD (Drill Data Example)

- **Example : Drill files for a 4 layer PCB**

drill.drl

```
%
T1C.006*/050
X02345Y0105
X0231Y0105
X02345Y0109
X02345Y0109
X02345Y0113
X0231Y0113
X02345Y0117
X0231Y0117
X02345Y0233
X0231Y0233
X0231Y0237
X02345Y0237
X02345Y0241
X0231Y0241
X02345Y0245
```

drill.lst

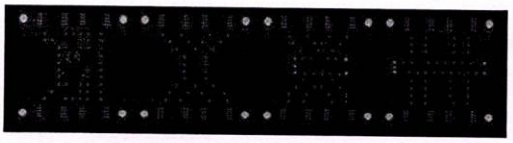
```
Drill Listing
*************
Drill: 006 Tool: 1 Feed: 0 Speed: 0
X 234500 Y 105000
X 231000 Y 105000
X 231000 Y 109000
X 234500 Y 109000
X 234500 Y 113000
X 231000 Y 113000
X 234500 Y 117000
X 231000 Y 117000
X 234500 Y 233000
X 231000 Y 233000
X 231000 Y 237000
X 234500 Y 237000
X 234500 Y 241000
X 231000 Y 241000
```

drill.rep

```
Drill Sizes Report
******************
Tool  Size  Pltd  Feed  Speed  Qty
****  ****  ****  ****  *****  ***
1     8     x     0     0      443
2     29    x     0     0      8
3     33    -     0     0      2
4     100   -     0     0      16
```


PCB CAD (Drill Data Example)

- **Example : Drill plot for a 4 layer PCB**
  - we can plot our drill data over the top of our GERBERS in order to see if the holes line up to check that everything is accurate.



PCB CAD (Drawings)

- **Fab & Drill Drawings**
  - in addition to the CAM files that you send to a PCB manufacturer, you also need to generate drawings so that the fab engineers can understand what you are trying to accomplish.
  - this provides an additional layer of checking.
  - there are two main types of drawing that accompany your CAM files:

Fabrication Drawing
- contains board outline dimensions.
- gives stackup dimensions, materials, surface finish.
- provides any special information about the board that the fab shop needs to know.

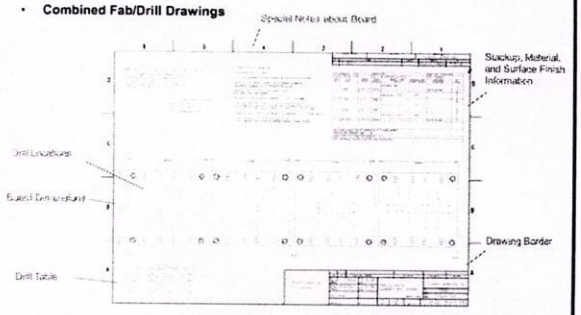
Drill Drawing
- contains a plot showing the location of each drill hole on the board
- contains a **drill table** listing the different drill sizes and their quantity

- a more common approach is to combine the two into a:

Combined Drill/Fab Drawing

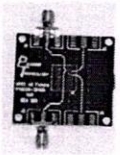
PCB CAD (Drawing Example)

- **Combined Fab/Drill Drawings**



PCB CAD (Example)

- **Final Result**
  - The Gerber, Drill, and Drawing files were sent to a fab shop and 1 week later the PCB arrived.



Design for Manufacturability

- **Design for Manufacturability (DFM)**
  - The physical sizes that we use in a PCB design are not arbitrary.
  - The minimum sizes and spacing are dictated by the Fabrication Vendor.
  - Prior to designing a PCB, you must look at the *Design Rules* for potential vendors and select the Design Rules that meet your application.
  - On a PCB, the smaller the features, the more circuitry that can fit on a board.
  - However, the smaller the feature, the higher the cost of the board.
  - In addition, when designing transmission lines, we select our material, widths, and spacing in order to achieve a characteristic impedance. Not necessarily the minimum geometry.
  - We are constantly trading off:

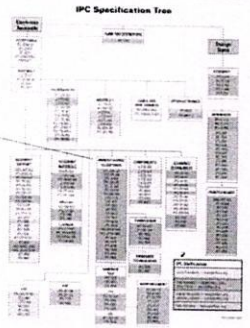
Electrical Performance vs. Mechanical Performance vs. Cost

Design for Manufacturability

- **IPC**
  - "Institute for Interconnecting and Packaging Electronic Circuits"
  - The organization that defines PCB standards
  - PCB Fab vendors will typically adhere to a particular IPC standard
  - This allows you to design your board using widths/spacing from an IPC standard that is independent of a PCB Fab vendor.
  - This way, your design can be sent to any Fab shop that supports that particular IPC standard.
  - IPC will work with a group of experts in the field and define the dimensions that can be achieved for a given standard. This way a standard is achievable by the majority of Fab Shops that are regularly improving their processes.

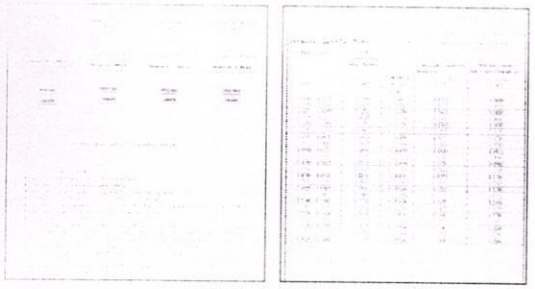
Design for Manufacturability

- **IPC**
  - IPC specs all aspects of electronic interconnect (PCB, Assembly, Materials, etc.)
  - The dimensions we are interested in are found in the "Printed Board / Acceptance" section:



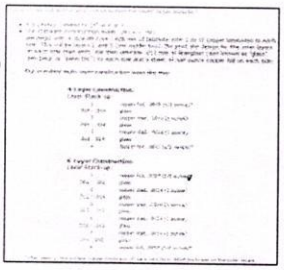
Design for Manufacturability

- **Vendor Specific Capabilities**
  - Here is an example of specifications from PCBexpress.com



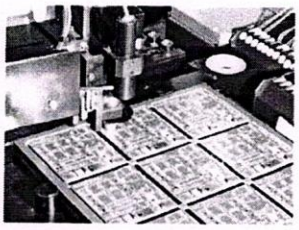
Design for Manufacturability

- **Vendor Specific Capabilities** (PCBexpress.com cont...)
  - notice that we can use trace widths as small as 0.006"
  - however, if we want to design a 50 ohm transmission line (i.e., a microstrip or stripline) we need to look at the stackup and materials in order to choose a width that gives us our desired impedance.



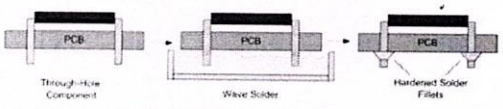
Component Loading

- **Loading**
  - In high volumes, PCBs are loaded using automatic assembly machines.
  - this is typically called "Pick and Place" which refers to the robotic arms *picking* up a component from a bin of parts and *placing* it on the PCB.



Through-Hole Component Loading

- **Through Hole**
  - Through-Hole Technology refers to components that have leads that extend all the way through the PCB.
  - When designing a PCB, a plated through-hole is created that is large enough to accept the leads of the part.
  - The leads of the part are then inserted into the holes.
  - The entire board is then ran through a *Wave Soldering* process which applies solder to the backside of the board.
  - The leads are then *trimmed* from the backside of the board.



SMT Component Loading

- **Surface Mount Technology**
  - SMT refers to components that only contact the surface of the board.
  - this allows components to be loaded without having to drill holes in the board.
  - this allows much smaller components to be used.
  - SMT technology can be used on both the top and bottom of the PCB (i.e., doubled sided PCAs)

SMT Component Loading

- **Solder Paste**
  - the first step in using automated SMT assembly is to apply *solder paste*.
  - solder paste is a mixture of solder and flux.
  - flux is an acid solution that eats through oxidation.
  - by mixing solder and flux together, a thick, viscous material is create (about the same viscosity as toothpaste).
  - this material is called *solder paste* and has some attractive properties:
    1) It can be applied to the pads of a PCB using a stencil since it is viscous
    2) It contains flux so any oxidation on the pads will be eliminated
    3) If a component is placed on the flux, the component will stick. The solder paste is sticky enough so that a PCB can be turned upside down and the components will not fall off.
  - The entire board is then heated up in a reflow oven. This burns the flux out of the paste leaving only molten solder. When the board is cooled, a solid solder joint is formed.

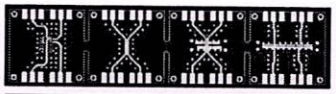
SMT Component Loading

- **Solder Paste**
  - if a board is to be loaded using automated SMT pick and place technology, the CAD tool must produce data for the paste stencil.

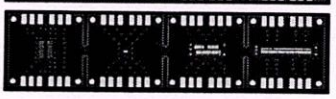
    top_paste.pho
    bottom_paste.pho

ex)

L1.pho

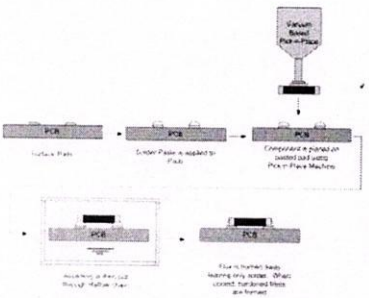


top_paste.pho



SMT Component Loading

- **SMT Process**



PCB Transmission Lines

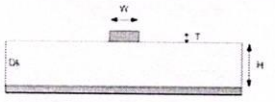
- **Transmission Lines**
  - We've seen that a transmission line is described in terms of Impedance and Prop Delay
  - We've also seen that the Characteristic Impedance and Prop Delay are only functions of the inductance and capacitance of the line:

$$Z_0 = \sqrt{\frac{L}{C}} \qquad T_D = \sqrt{LC}$$

  - Inductance and capacitance are frequency independent and functions of the structure geometries and materials.
  - This means that for a transmission line, Z_0 and T_D are only dependent on the physical shape and material properties.
  - We use the term ***Controlled Impedance*** to describe T-line structures where we define a geometry in which we know exactly where the signal and return current propogate.

PCB Transmission Lines

- **Microstrip**
  - A microstrip transmission line consists of a signal trace residing over an *infinite* ground plane.
  - On a PCB, these transmission lines exist when you use the outer layers for signal traces and then put a *plane* beneath (typically directly beneath, L2)
  - The return path is the ground plane beneath the trace.
  - NOTE: There are two important things to notice about a Microstrip:
    1) The field lines are NOT completely contained within a homogenous medium so there is no FEXT canceling.
    2) The field lines extend upward from the signal trace and can coupled to adjacent boards.

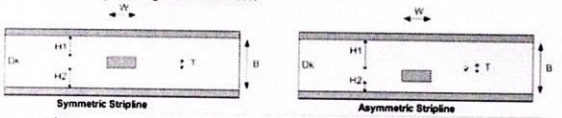


PCB Transmission Lines

- **Embedded Microstrip**
  - This is simply a microstrip that is buried within the dielectric
  - This type of structure attempts to contain all of the field lines within the same dielectric material.

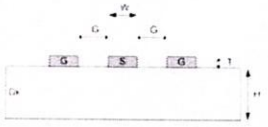
PCB Transmission Lines

- **Stripline**
  - A stripline transmission line consists of a signal trace sandwiched between two return planes
  - On a PCB, these transmission lines exist on inner layers if you are able to put planes above and beneath the signal layer (typically requires at least 6 layers)
  - The return path is split between the two ground planes.
  - NOTE: There are two important things to notice about a Stripline:
    1) The field lines ARE completely contained within a homogenous medium so there is FEXT canceling.
    2) The field lines are strongly coupled to the two ground planes so coupling to adjacent neighbors is minimized.



PCB Transmission Lines

- **Coplanar**
  - A coplanar transmission line uses the same metal layer of the PCB for both the signal and return.
  - this is commonly used on PCB's with very few layers.



Signal Integrity on PCBs

- **Impedance Discontinuities in PCB's**
  - sources of impedance discontinuities on PCB's

1) Vias	(typically larger than the traces we use)
2) Pads	(typically larger than the traces we use)
3) Cross-talk	(coupling to other traces causes Z_0 to change)
4) Return Path	(switch routing layers also requires a change in the return path)
5) Dk variance	(Dk can change from one region of the board to another)
6) Etching Tolerance	(Trace widths will have tolerances, +/-x%, that changes Z_0)
7) Etching Variance	(Trace widths can change due to etching variance across the board)
8) Plating Variance	(The thickness of a trace can chance across the board due to plating)
9) Thickness Variance	(The lamination may result in different board thicknesses vs. location)

  - each of these noise sources must be analyzed in the noise budget.

K.S.R.M. COLLEGE OF ENGINEERING

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Certificate of Completion

This is to certify that

Mr/Ms. B. Sivaraj

Bearing the Roll No 17941A0204

has Succesfully completed certification course on

PCB Design

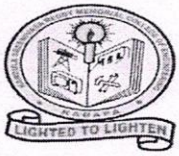
From 17/05/2021 ***to*** 22/05/21 , ***Organized by Department of***

Electrical & Electronics Engineering.

Kalyani
Coordinator

Ugwaly
Head Of Department

V. S. S. Murthy
Principal



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Department of Electrical and Electronics Engineering

Certification Course on PCB Design

Feedback Form

S.No	Roll List	Name of the Student	Is the Course content meet your expectation	Is the lecture sequence well planned	Is the level of course high	Is the course exposed you to the new knowledge	Rate the Knowledge of the Speaker	Rate the value of Course in increasing your skills
1	179Y1A0204	BANDA SIVARAJ	Agree	Strongly Agree	Yes	4	5	Nil
2	179Y1A0206	BHUMIREDDY CHANDRAKALA (W)	Agree	Strongly Agree	Yes	5	4	Nil
3	179Y1A0207	DUGGISETTY JAGAPATHI BABU	Agree	Strongly Agree	Yes	4	5	Nil
4	179Y1A0208	GADDAM ANIL KUMAR	Agree	Strongly Agree	Yes	5	4	Nil
5	179Y1A0209	GAJJALAKONDUGARI RENUKA DEVI (W)	Agree	Strongly Agree	Yes	4	5	Nil
6	179Y1A0210	GORANTLA SASIDHAR	Agree	Strongly Agree	Yes	5	4	Nil
7	179Y1A0211	KRISHNAM SNEHALATHA (W)	Agree	Strongly Agree	Yes	5	4	Nil
8	179Y1A0212	KURUBA LAKSHMIKANTH	Agree	Strongly Agree	Yes	4	5	Nil
9	179Y1A0214	MANCHALA SOWMYA (W)	Agree	Strongly Agree	Yes	5	4	Nil
10	179Y1A0215	MAYANA ABDUL SUHAIB KHAN	Agree	Strongly Agree	Yes	4	5	Nil
11	179Y1A0216	MEDA SANDEEP	Agree	Strongly Agree	Yes	5	4	Nil
12	179Y1A0217	MEKALA GANGADHARA	Agree	Strongly Agree	Yes	4	5	Nil

13	179Y1A0218	NAKKALAPALLI SHIREESHA (W)	Agree	Strongly Agree	Yes	5	4	Nil
14	179Y1A0219	POSA VENKATA SREEVALLI (W)	Agree	Strongly Agree	Yes	5	4	Nil
15	179Y1A0220	PASUPULETI GAYATHRI DEVI (W)	Agree	Strongly Agree	Yes	4	5	Nil
16	179Y1A0221	RAYAPU VENNELA (W)	Agree	Strongly Agree	Yes	4	5	Nil
17	179Y1A0222	SANNAPURI VENKATESH	Agree	Strongly Agree	Yes	5	4	Nil
18	179Y1A0223	SHAIK ABDUL FAROOQ	Agree	Strongly Agree	Yes	4	5	Nil
19	179Y1A0224	SHAIK MISBA SANIA (W)	Agree	Strongly Agree	Yes	5	4	Nil
20	179Y1A0225	SUCHARITHA PANYAM (W)	Agree	Strongly Agree	Yes	4	5	Nil
21	179Y1A0226	SYED AZARUDDIN	Agree	Strongly Agree	Yes	5	4	Nil
22	179Y1A0227	SYED HAFEEZ PARVEZ	Agree	Strongly Agree	Yes	5	4	Nil
23	179Y1A0228	SYED SHAZIA TABASSUM	Agree	Strongly Agree	Yes	5	4	Nil
24	179Y1A0230	YARRANAGU RAJESH REDDY	Agree	Strongly Agree	Yes	4	5	Nil
25	189Y5A0201	ATHINJERI RAJESH	Agree	Strongly Agree	Yes	5	4	Nil
26	189Y5A0202	BIJIVEMULA SUDARSHAN REDDY	Agree	Strongly Agree	Yes	4	5	Nil
27	189Y5A0203	BILLIPATI PAVAN KUMAR	Agree	Strongly Agree	Yes	5	4	Nil
28	189Y5A0204	BOLLINENI PRASANNA LAKSHMI	Agree	Strongly Agree	Yes	4	5	Nil

29	189Y5A0205	CHABUK SAWAR MOHAMMED SUBHAN	Agree	Strongly Agree	Yes	5	4	Nil
30	189Y5A0206	CHUNDU NIRANKUMAR	Agree	Strongly Agree	Yes	4	5	Nil
31	189Y5A0207	DARA PRAVEEN	Agree	Strongly Agree	Yes	5	4	Nil
32	189Y5A0208	DASARI KISHOR KUMAR	Agree	Strongly Agree	Yes	4	5	Nil
33	189Y5A0209	DASARI PAVAN KALYAN	Agree	Strongly Agree	Yes	5	4	Nil
34	189Y5A0210	DWARSALA VEERA MADHAVI (W)	Agree	Strongly Agree	Yes	4	5	Nil
35	189Y5A0211	GOSALA SRINIVASA RAO	Agree	Strongly Agree	Yes	5	4	Nil
36	189Y5A0212	GUNDLAMADUGU REDDY KRISHNA	Agree	Strongly Agree	Yes	4	5	Nil
37	189Y5A0217	KAPA OMKAR REDDY	Agree	Strongly Agree	Yes	5	4	Nil
38	189Y5A0218	KARAPUREDDY MANOJ KUMAR REDDY	Agree	Strongly Agree	Yes	4	5	Nil
39	189Y5A0219	KODURU KUMAR	Agree	Strongly Agree	Yes	5	4	Nil
40	189Y5A0220	KONANGI CHANDU	Agree	Strongly Agree	Yes	4	5	Nil
41	189Y5A0221	KOTHAPALLI SOMANJU	Agree	Strongly Agree	Yes	5	4	Nil
42	189Y5A0222	KUMARAKALVA BALAJI	Agree	Strongly Agree	Yes	4	5	Nil
43	189Y5A0223	KUMMARA VISHNU	Agree	Strongly Agree	Yes	5	4	Nil
44	189Y5A0224	KUNDALA SIVASAI	Agree	Strongly Agree	Yes	4	5	Nil
45	189Y5A0227	KUSAM CHANDRA PRAKASH REDDY	Agree	Strongly Agree	Yes	5	4	Nil
46	189Y5A0228	LAKKIREDDY MADHU SAI	Agree	Strongly Agree	Yes	4	5	Nil

47	189Y5A0229	LAVANUR REVANTH REDDY	Agree	Strongly Agree	Yes	5	4	Nil
48	189Y5A0230	L. SAI HARSHINI	Agree	Strongly Agree	Yes	4	5	Nil
49	189Y5A0231	MOGHAL ASLAM BAIG	Agree	Strongly Agree	Yes	5	4	Nil
50	189Y5A0232	MOOLA PRADEEP KUMAR REDDY	Agree	Strongly Agree	Yes	4	5	Nil
51	189Y5A0233	MULE SIVA JYOTHSNA	Agree	Strongly Agree	Yes	5	4	Nil
52	189Y5A0234	NEELAM PAVAN KUMAR REDDY	Agree	Strongly Agree	Yes	4	5	Nil
53	189Y5A0241	PULLIRUPU SATHISH KUMAR	Agree	Strongly Agree	Yes	5	4	Nil
54	189Y5A0242	RAJOLI KARTHIK REDDY	Agree	Strongly Agree	Yes	4	5	Nil
56	189Y5A0243	RAMIREDDY PAVAN KUMAR REDDY	Agree	Strongly Agree	Yes	5	4	Nil
57	189Y5A0244	REPALLE ANOK	Agree	Strongly Agree	Yes	4	5	Nil
58	189Y5A0245	SARASWATHI MADHURIMA	Agree	Strongly Agree	Yes	5	4	Nil
59	189Y5A0246	SAREDDY NIRANJAN REDDY	Agree	Strongly Agree	Yes	4	5	Nil
60	189Y5A0247	SHAIK AHAMMAD	Agree	Strongly Agree	Yes	5	4	Nil
61	189Y5A0252	SULTHAN SAHEB KAMAL BASHA	Agree	Strongly Agree	Yes	4	5	Nil

K. Kalyan Kumar
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